PLEASE AMEND THE CLAIMS AS FOLLOWS:

Please cancel Claims 26-28

29. A semiconductor device structure comprising:

a semiconductor substrate having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure , wherein said upper metal lines are substantially thicker than said lower metal lines.

24 88. A semiconductor device structure comprising:

a semiconductor substrate having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure, wherein said upper metal lines are substantially wider than said lower metal lines.

25 89. A semiconductor device structure comprising:

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a semiconductor substrate having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines in layers, separated by inorganic intermetal dielectric layers, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, separated by organic dielectric layers, connected to said interconnecting metallization structure, wherein said organic dielectric layers are thicker than said inorganic intermetal dielectric layers.

Please cancel non-elected claims 90-99.